REMARKS

Claims 1-26 were rejected under 35 U.S.C. 102(b) as being anticipated by Li *et al.* (U.S. Patent No. 6,208,183). That rejection is respectfully traversed and reconsideration is requested. Although applicants could swear behind the Li *et al.* reference, we have not done so because the claims distinguish the reference for the reasons discussed below.

An embodiment of a clock multiplier of the present invention, particularly as applied to a data communications circuit, is illustrated in Fig. 5. A delay line 142 receives a reference clock rclk and a multiplied clock bclk at respective times to generate the clock bclk. The delay of the delay line 142 is controlled by phase comparison of the generated clock bclk and the reference clock rclk in a phase comparator 147. Note, however, that bclk and rclk are of different frequencies and are thus not readily compared. A prior technique illustrated in Fig. 2 relied on a frequency divider to generate a signal dclk from the multiplied signal bclk of the same frequency as the reference rclk for appropriate comparison. However, the frequency divider introduced a phase offset. With the present invention, the two signals are directly compared for a precise phase comparison without phase offset introduced by either signal. To that end, control 145 provides a control signal 146 to the phase comparator such that the phase comparison is only made at an edge of the slower clock rclk.

It is also significant that the phase comparator 147 is a proportional phase comparator. Consider the operation of a non-proportional phase comparator as illustrated in Fig. 19. The phase comparator output is shown at the bottom of the figure. At each point of comparison, once every four cycles, the phase comparator output toggles. It holds the output at either of the two output levels for the duration of the next four cycles. By comparison, note the proportional outputs down and up in Figs. 8 and 9 of this application. The durations of the output pulses up and down are directly proportional to the phase differences between the signals bclk and rclk. By providing this proportional output, the dither of prior art multiplying DLLs is overcome by eliminating the oscillation of the control voltage about its proper value.

See pages 7 and 8 of the specification for a discussion of both the direct phase comparison and the proportional phase comparator. In particular, note page 8, lines 23-25.

Li *et al.* does rely on a delay line and a phase comparator to control that delay line. However, Li *et al.* does not compare the reference clock CLK_{REF} with the output clock CLK_{OUT}, but rather with a frequency divided signal CLK^{*}_{OUT}. As in the prior art of Fig. 2 of the present application, Li *et al.* relies on a frequency divider 208 to compare two signals of the same frequency rather than using a technique, such as the windowing technique described in the embodiments of the present invention, to directly compare the two signals of different frequencies. The frequency divider 208 introduces a phase offset between the multiplied output clock and the reference clock.

A major advantage of the claimed multiplier is that it directly compares the reference clock with the multiplied clock, and thus precisely aligns these two signals that are being multiplexed onto the delay line. This precise alignment allows this approach to be used in applications that require low jitter. To make this distinction more clear, the independent claims have been amended to insert the term "direct." The frequency divider 208 of Li *et al.* prevents a direct comparison of the multiplied clock and the reference clock.

Li *et al.* also does not state that the phase/frequency detector 202 is proportional. See column 7, lines 32-42. Thus, Claims 1, 7-10, 14 and 20-23 further distinguish Li *et al.* on that basis.

Regarding Claims 2, 3, 8, 9, 15, 16, 21, and 22, the Li *et al.* patent makes no mention of the phase offset of the phase comparator 202. The passage in column 7 makes no mention of phase offset but merely recites the basic function of an edge-triggered phase comparator. In fact, since the reference clock is delayed in delay 214 and the output clock is divided in divider 208 in the system of Li *et al.*, so much phase error is introduced that the phase offset of the phase comparator is most likely not an issue.

Regarding Claims 4, 10, 17, and 23, the system of the Li *et al.* patent uses a separate phase comparator 202 and charge pump 204. It does not use a combined phase comparator and charge pump circuit as, for example, described in U.S. Patent 6,275,072, referenced at page 8 of the specification.

Information Disclosure Statement

An Information Disclosure Statement (IDS) is being filed concurrently herewith. Entry of the IDS is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____

James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
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